Digital Signal Processors

Powerful special purpose 8/16/32 bit microprocessors designed to meet the computational demands and power constraints of typical applications like image processing, multimedia, audio, video, HDTV, DSP modem and telecommunication processing systems.They achieve high speed typically by implementing algorithms in hardware whereas GPPs implement the algorithm in software and the speed of execution depends primarily on the clock for the processors.DSPs also find use in systems for recognizing an image pattern or a DNA sequence fast. The DSP as a GPP is a single chip VLSI unit that possesses the computational capabilities of a microprocessor and also has a Multiply and Accumulate (MAC) unit(s). Nowadays, a typical DSP has a 16 x 32 MAC unit. A DSP provides fast, discrete-time, signal-processing instructions with Very Large Instruction Word (VLIW) processing capabilities.
A typical DSP includes following key units:

- Program memory: For storing the program required by DSP to process the data.
- Data memory: Working memory for storing temporary variables and data/signal to be processed.
- Computational engine: Performs the signal processing in accordance with the stored program. The computational engine incorporates many specialized arithmetic units and each of them operates simultaneously to increase the execution speed. It also includes multiple hardware shifters for shifting operands and saves execution time.
- I/O unit: It acts as an interface between the outside world and DSP. It is responsible for capturing signals to be processed and delivering the processed signals.

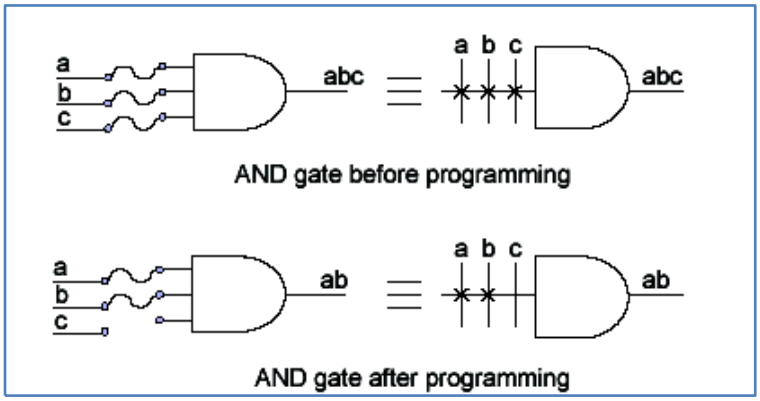
Application Specific Integrated Circuits (ASIC)

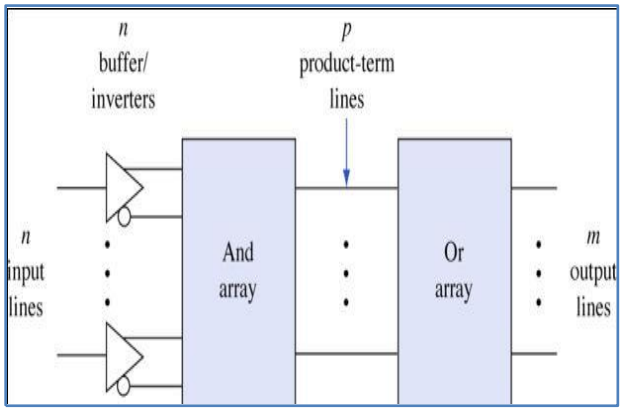
ASICs is a microchip design to perform a specific and unique function typically using a single chip which integrates several functions. There by reduces the system development cost. Most of the ASICs are proprietary (which having some trade name) and are referred as Application Specific Standard Products or Application Specific System Processors (ASSP).

A Typical Application of ASIC/ASSP:
Assume that there is an embedded system that interconnects using a specific protocol to another remote system. Also, assume that there is a need for suitable encryption and decryption. For these tasks, besides embedding the software, it may also be necessary to embed some RTOS features. If the

software alone is used for the above tasks, it may take a longer time than a hardwired solution for application-specific processing. An ASSP chip provides a better solution. For example, an ASSP chip [from i2Chip (http://www.i2Chip.com)] has a TCP, UDP, IP, ARP, and Ethernet 10/100 MAC (Media Access Control) hardwired logic included into it. The chip from i2Chip, W3100A, is a unique hardwired Internet connectivity solution. Much needed TCP/IP stack processing software for networking tasks is thus available as a hardwired solution. This gives output five times faster than a software solution using the system's GPP. It is also an RTOS-less solution.
Using the same microcontroller in the embedded system to which this ASSP chip interfaces, Ethernet connectivity can be added easily.

Programmable logic devices(PLD's)
PLD is an electronic component that contains large numbers of gates, flip-flops, etc. that can be configured by the user to perform different functions. It is used to build digital circuits which are reconfigurable. A logic gate has a fixed function but a PLD does not have a defined function at the time of manufacture.PLDs are typically built with an array of AND gates (AND-array) and an array of OR gates (OR-array)





One of the simplest programming technologies is to use fuses. In the original state of the device, all the fuses are intact.Programming the device involves blowing those fuses along the paths that must be removed in order to obtain the particular configuration of the desired logic function.
Advantages of using PLDs are less board space, faster, lower power requirements (i.e., smaller power supplies), less costly assembly processes, higher reliability (fewer ICs and circuit connections means easier troubleshooting), and availability of design software.
Based on the interconnections, complexity, and whether the AND array or the OR array is programmable, PLDs are categorized as follows:

1. SPLDs (Simple Programmable Logic Devices)

- *PROM (Programmable Read-Only Memory):* Has a fixed AND array (constructed as a decoder) and programmable connections for the output OR gates array.The PROM implements Boolean functions in sum-of-minterms form.
- PAL (Programmable Array Logic): The PAL device is a PLD with a fixed OR array and a programmable AND array.
- PLA (Programmable Logic Array): Instead of using a decoder as in PROMs, a number (k) of AND gates is used where $k < 2^n$, (n is the number of inputs).Each of the AND gates can be programmed to generate a product term of the input variables and does not generate all the minterms as in the ROM.The AND and OR gates inside the PLA are initially fabricated with the links (fuses) among them.The specific Boolean functions are implemented in sum of products form by opening appropriate links and leaving the desired connections.

2. CPLD (Complex Programmable Logic Device)

A CPLD contains a bunch of PLD blocks whose inputs and outputs are connected together by a global interconnection matrix. Thus a CPLD has two levels of programmability. Each PLD block can be programmed and then the interconnections between the PLDs can be programmed.

- FPGA (Field-Programmable Gate Array):

FPGA is an integrated circuit that contains many (64 to over 10,000) identical logic cells that can be viewed as standard components. Each logic cell can independently take on any one of a limited set of personalities.Individual cells are interconnected by a matrix of wires and programmable switches. A user's design is implemented by specifying the simple logic function for each cell and selectively closing the switches in the interconnect matrix.
Array of logic cells and interconnect form a fabric of basic building blocks for logic circuits. Complex designs are created by combining these basic blocks to create the desired circuit.

Commercial off-the-shelf components (COTs)

A Commercial off the Shelf product is one which is used as it is.The COTS component may be developed around a general purpose or domain specific processor or an ASICs or a PLD.The major advantage of using COTS is that they are readily available in the market, and a developer can cut down his/her development time to a great extent.For example: To incorporate a motion sensing module for self balancing of a robot, a designer can use the 3-Axis Accelerometer Sensor based on MMA7660FC with an I^2C interface sold by Rhydolabz.

The major drawback of using COTS components in embedded design is that the manufacturer of the COTS component may follow a non-operational and non-standard manufacturing. Further, a manufacturer may withdraw the product or discontinue the production of the COTS at any time if rapid change in technology occurs