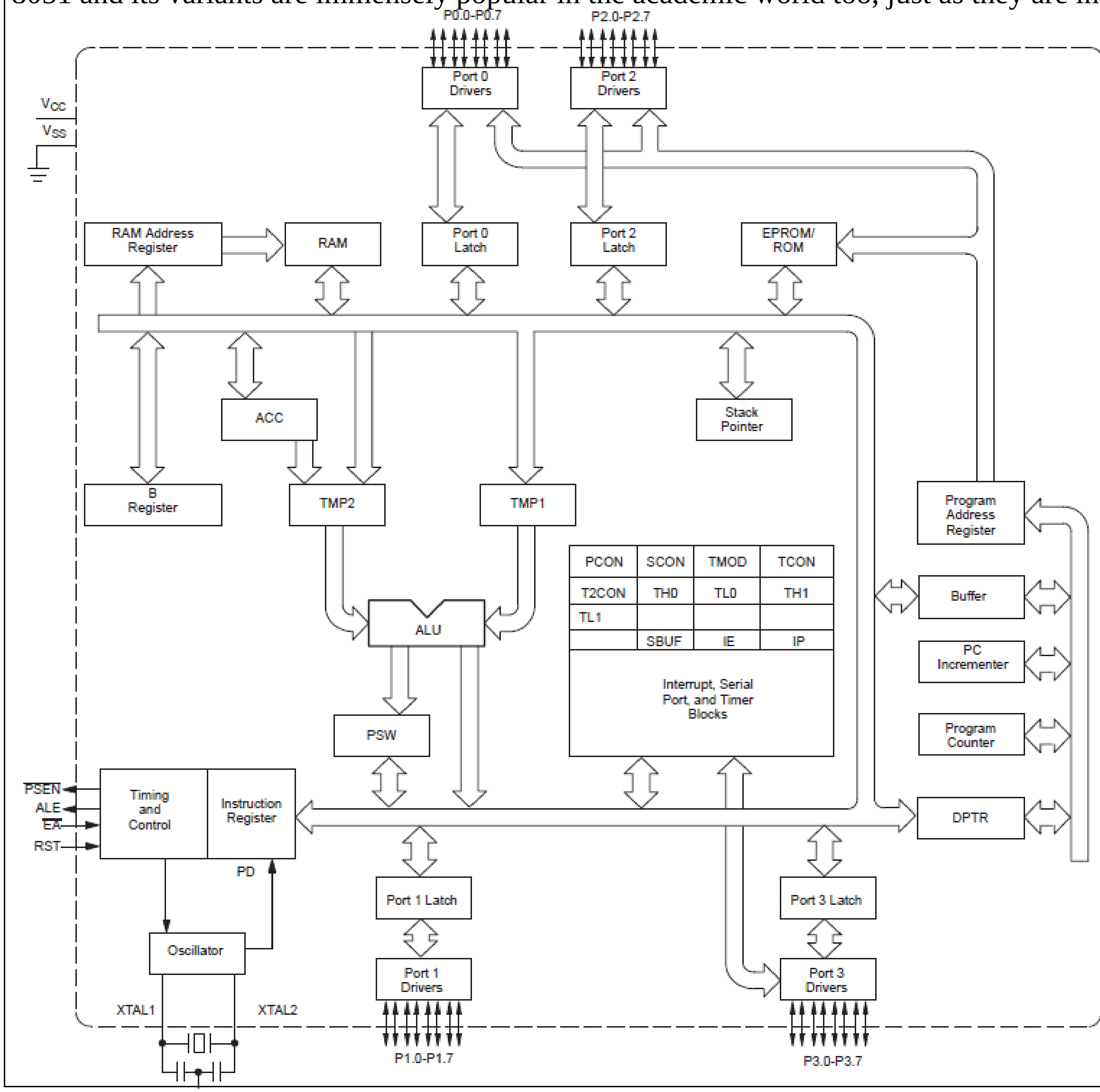
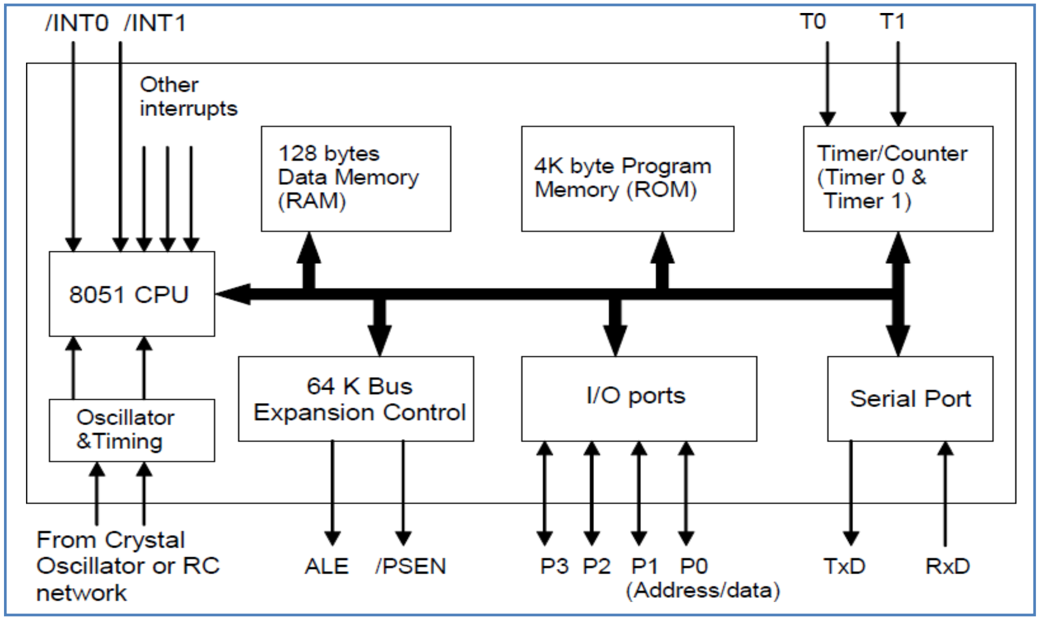
8051 Microcontroller

Intel introduced 8051, referred as MCS-51, in 1981 as an 8-bit processor.
Several chip vendors have extended 8051 to incorporate advanced features, numerous additional peripherals and extra memory.
The 8051 Family is one of the fastest growing microcontroller architectures in the world of electronics today.
There are over 400 device variants of 8051 from various silicon vendors like Silicon Laboratories, Philips, Amtel, Dallas and Infineon to name a few.
8051 and its variants are immensely popular in the academic world too, just as they are in the arena of industrial applications.



Feature	8051	8052	8031
ROM (on chip)	4K	8K	-
RAM (bytes)	128	256	128
Timers	2	3	2
I/O pins	32	32	32
Serial Port	1	1	1
Interrupt Sources	5	8	6



Salient features of 8051 microcontroller are given below.

- Eight bit CPU
- On chip clock oscillator
- 4Kbytes of internal program memory (code memory) *[ROM]*
- 128 bytes of internal data memory *[RAM]*
- 64 Kbytes of external program memory address space.
- 64 Kbytes of external data memory address space.
- 32 bi directional I/O lines (can be used as four 8 bit ports or 32 individually addressable I/O lines)
- Two 16 Bit Timer/Counter :T0, T1
- Full Duplex serial data receiver/transmitter
- Four Register banks with 8 registers in each bank.
- Sixteen bit Program counter (PC) and a data pointer (DPTR)
- 8 Bit Program Status Word (PSW)
- 8 Bit Stack Pointer

- Five vector interrupt structure (RESET not considered as an interrupt.)
- 8051 CPU consists of 8 bit ALU with associated registers like accumulator 'A' , B register, PSW, SP, 16 bit program counter, stack pointer.
- ALU can perform arithmetic and logic functions on 8 bit variables.
- 8051 has 128 bytes of internal RAM which is divided into
  - Working registers [00 – 1F]
  - Bit addressable memory area [20 – 2F]
  - General purpose memory area (Scratch pad memory) [30-7F]

Component	Number/Count	Size	Register(s)	Address (hex)
CPU with Registers	1 CPU, 2 Registers	8bit	A and B	E0 and F0
Program Counter and data pointer	1	16bit	PC and DPTR	82-83
Program Status Word	1	8bit	PSW	D0
Stack Pointer	1	8bit	SP	81
Internal ROM	1	4K	-	
Internal RAM	1	128bytes	-	
Register Banks	4	8bit		00-1F
Bit Addressable Memory	1	16bytes	-	20-2F
General Purpose Data Memory	1	80bytes	-	30-7F
I/O ports	4	8bit	P0-P3	80, 90, A0 and B0
Timers/Counters	2	16bit	T0 and T1	90-91 and 92-93
Full Duplex Serial Data Receiver/Transmitter	1	8bit	SBUF	99
Control Registers	6		TCON, TMOD, SCON, PCON, IP and IE	88, 89,98,87, B8 and A8
Interrupt Sources	2 external, 3 internal			
Oscillator and Clock Circuits	1			
Expansion Bus Control	1	64K		

Special Function Registers (SFRs)

A special area of the on-chip memory.The functions of the SFRs are described in the text that follows.

Accumulator:

ACC is the Accumulator register. The mnemonics for Accumulator- Specific instructions, however, refer to the Accumulator simply as A.

Used for storing intermediate results obtained during operation.

Results obtained from arithmetic operations performed by ALU are stored here.

Data to be moved from one register to another must go through the accumulator

B Register:

The B register is used during multiply and divide operations.

For other instructions it can be treated as another scratch pad register.

Stack Pointer:

The Stack Pointer register is 8 bits wide.

It is incremented before data is stored during PUSH and CALL executions.

While the stack may reside anywhere in on-chip RAM, the Stack Pointer is initialized to 07H after a reset. This causes the stack to begin at locations 08H (can be changed).

Data Pointer:

The Data Pointer (DPTR) consists of a high byte (DPH) and a low byte (DPL).

Its intended function is to hold a 16-bit address (usually to point to the data within the program segment or for accessing the external memory).

It may be manipulated as a 16-bit register or as two independent 8-bit registers.

Ports 0 to 3:

P0, P1, P2, and P3 are the SFR latches of Ports 0, 1, 2, and 3, respectively.

Writing a one to a bit of a port SFR (P0, P1, P2, or P3) causes the corresponding port output pin to switch high.

Writing a zero causes the port output pin to switch low.

When used as an input, the external state of a port pin will be held in the port SFR (i.e., if the external state of a pin is low, the corresponding port SFR bit will contain a 0; if it is high, the bit will contain a 1).

Timer Registers:

The basic 8051 contains two 16-bit timer/counters for timing intervals or counting events.

Timer 0 is located at addresses 8AH (TL0, low byte) and 8CH (TH0, high byte) and Timer 1 is located at addresses 8BH (TL1, low byte) and 8DH (TH1, high byte).

The Timer Mode register (TMOD), which is located at address 89H, and the Timer Control register (TCON)$^{\text{bit addressable}}$, which is located at address 88H, are used to program the timeroperations.

Serial Communication Registers:

The 8051 contains an on-chip serial port for communication with serial devices such as modems or for interfacing with other peripheral devices with a serial interface (A/D converters, RF/IR transmitters, etc).

The Serial Data Buffer register (SBUF) located at address 99H holds both the transmit data and the receive data.

Writing to SBUF loads data for transmission while reading SBUF returns the received data.

The Serial Buffer is actually two separate registers, a transmit buffer and a receive buffer each 8bits.

When data is moved to SBUF, it goes to the transmit buffer and is held for serial transmission. (Moving a byte to SBUF is what initiates the transmission.)

When data is moved from SBUF, it comes from the receive buffer.

Various modes of operation are programmable through the bit- addressable Serial port Control register (SCON), which is located at address 98H.

Interrupt Management Registers:

The 8051 has 5 interrupt sources which include 2 external interrupts, 2 timer interrupts and a serial port interrupt.

Each interrupt can be individually enabled or disabled by writing a ‘1’ or a ‘0’ respectively into the Interrupt Enable register (IE).

The bit 7 of the register is a global enable bit, which if cleared, will disable all interrupts.

In addition, each interrupt source can be set to either one of the two priority levels i.e. High or Low.

This is done through the Interrupt Priority register (IP), which is located at address B8H.

Program Status Word:

The PSW register contains program status information as detailed in the figure.

MSB							LSB
CY	AC	F0	RS1	RS0	OV	—	P

Bit	Symbol	Functions
PSW.7	CY N	Carry Flag-Set if there is a carry out of bit 7 during an addition operation or Set if there is a borrow into bit 7 during a subtraction operation
PSW.6	AC O	Auxiliary Carry flag (for BCD operations)- Set if a carry was generated out of bit 3 into bit 4 or if the result in the lower nibble is in the range 0AH to 0FH
PSW.5	F0 T	Flag 0. (Available to the user for general purposes.)
PSW.4	RS1 E	Register Bank Select control bit 1
PSW.3	RS0 :	Register Bank Select control bit 1
PSW.2	OV T	Overflow Flag-set after an addition or subtraction operation if there is an arithmetic overflow
PSW.1	- h	User-definable Flag
PSW.0	Parity Flaeg	Indicate an odd/even number of 1s in the ACC

Contents of (RS1, RS0) enable the working register banks as follows:

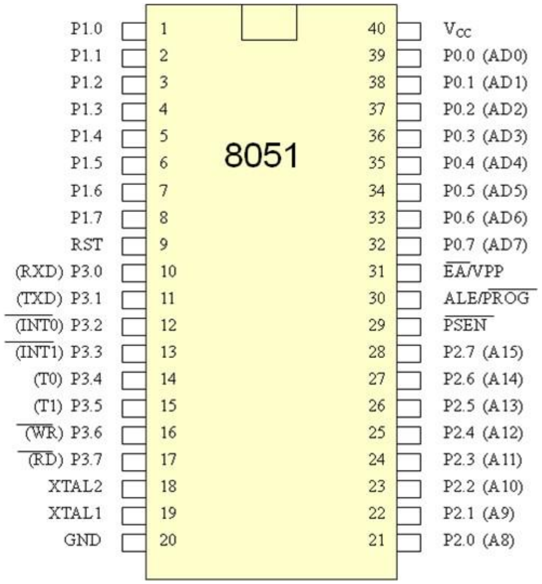
(0,0)— Bank 0 (00H–07H)

(0,1)— Bank 1 (08H–0fH)

(1,0)— Bank 2 (10H–17H)

(1,1)— Bank 3 (18H–17H)

PIN DIAGRAM



Pins 1-8	**PORT 1**. Each of these pins can be configured as an input or an output.
Pin 9	**RESET**. A logic one on this pin disables the microcontroller and clears the contents of most registers. In other words, the positive voltage on this pin resets the microcontroller. By applying logic zero to this pin, the program starts execution from the beginning.
Pins10-17	**PORT 3**. Similar to port 1, each of these pins can serve as general input or output. Besides, all of them have alternative functions
Pin 10	**RXD.** Serial asynchronous communication input or Serial synchronous communication output.
Pin 11	**TXD.** Serial asynchronous communication output or Serial synchronous communication clock output.

Pin 12	**INT0.**External Interrupt 0 input
Pin 13	**INT1.** External Interrupt 1 input
Pin 14	**T0.** Counter 0 clock input
Pin 15	**T1.** Counter 1 clock input
Pin 16	**WR.** Write to external (additional) RAM
Pin 17	**RD.** Read from external RAM
Pin 18, 19	**XTAL2, XTAL1**. Internal oscillator input and output. A quartz crystal which specifies operating frequency is usually connected to these pins.
Pin 20	**GND.** Ground**.**
Pin 21-28	**Port 2.** If there is no intention to use external memory then these port pins are configured as general inputs/outputs. In case external memory is used, the higher address byte, i.e. addresses A8-A15 will appear on this port. Even though memory with capacity of 64Kb is not used, which means that not all eight port bits are used for its addressing, the rest of them are not available as inputs/outputs.
Pin 29	**PSEN.** If external ROM is used for storing program then a logic zero (0) appears on it every time the microcontroller reads a byte from memory.
Pin 30	**ALE**. Prior to reading from external memory, the microcontroller puts the lower address byte (A0-A7) on P0 and activates the ALE output. After receiving signal from the ALE pin, the external latch latches the state of P0 and uses it as a memory chip address. Immediately after that, the ALE pin is returned its previous logic state and P0 is now used as a Data Bus.
Pin 31	**EA.** By applying logic zero to this pin, P2 and P3 are used for data and address transmission with no regard to whether there is internal memory or not. It means that even there is a program written to the microcontroller, it will not be executed. Instead, the program written to external ROM will be executed. By applying logic one to the EA pin, the microcontroller will use both memories, first internal then external (if exists).

Pin 32-39	**PORT 0.** Similar to P2, if external memory is not used, these pins can be used as general inputs/outputs. Otherwise, P0 is configured as address output (A0-A7) when the ALE pin is driven high (1) or as data output (Data Bus) when the ALE pin is driven low (0).
Pin 40	**VCC.** +5V power supply.